

What is claimed is:

1. A semiconductor device, comprising
 - 5 a substrate;
 - an active area formed within the substrate;
 - a first non-planar metallization level which is formed
10 on the substrate and is in contact with the active area; and
 - a second planar metallization level arranged spaced
15 apart from the first metallization level above the substrate and connected to the first metallization level via a through connection.
2. The semiconductor device according to claim 1, wherein
20 the semiconductor device includes a field effect transistor having a gate, a source area and a drain area, wherein the first non-planar metallization level includes a first portion connected to the source area, a second portion connected to the drain area and a
25 third portion at least partially covering the gate, and wherein the second planar metallization level includes at least one portion connected to the first portion of the first non-planar metallization level or to the second portion of the first non-planar metallization level.
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3. The semiconductor device according to claim 2, wherein
the first portion and the third portion of the first non-planar metallization level are connected.
- 35 4. The semiconductor device according to claim 2, wherein
between the first non-planar metallization level and the second planar metallization level an insulating layer is arranged, wherein in the insulating layer at

least one through connection for a connection of the first non-planar metallization level to the second planar metallization level is formed.

- 5 5. The semiconductor device according to claim 2, wherein the third portion is implemented to shield the gate against electrostatic or electrodynamic interferences.
6. An amplifier circuit comprising a field effect
- 10 transistor according to claim 2.